REMARKS

Status of the Claims

Claims 1-6 are pending in the application, with Claims 1 and 4 being independent.

Requested Action

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the following remarks.

Claim Rejections

Claims 1, 2, 4, and 5 are rejected under 35 U.S.C. § 103 over U.S. Patent No. 5,812,191 (Orava et al.) in view of U.S. Patent No. 7,098,950 B2 (Yamamoto et al.). Claims 3 and 6 are rejected under 35 U.S.C. § 103 over the patent to Orava et al. in view of the patent to Yamamoto et al. and U.S. Patent No. 6,163,024 (Kozuka et al.).

Response to Rejections

These rejections are traversed for the following reasons.

Independent Claim 1 relates to an image pickup apparatus in which a pixel area, including a plurality of pixels each having a photoelectric conversion portion and a common output portion configured to sequentially amplify and output signals from the plurality of pixels included in the pixel area, is formed on a single semiconductor substrate. The apparatus comprises a power supply unit and a control circuit. The power supply unit is configured to effect power supply control of the common output portion independently of control of the power supply to the pixel area. The control circuit is configured to

effect control to supply no power to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and to supply power to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion.

Independent Claim 4 relates to an image pickup apparatus in which a pixel area, including an arrangement of a plurality of pixels each having a photoelectric conversion portion and a common output portion configured to sequentially amplify and output signals from the plurality of pixels included in the pixel area, is formed on a single semiconductor substrate. The apparatus comprises a power supply unit and a control circuit. The power supply unit is configured to supply a first power level and a second power level lower than the first power level to the common output portion. The control circuit is configured to effect control to supply power of the second power level to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and supply the first power level to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion.

In contrast, the citations to Orava et al. and Yamamoto et al. are not understood to disclose or suggest a control circuit configured to effect control to supply no power to a common output portion (of a plurality of pixels each having a photoelectric conversion portion and the common output portion) to which power supply is effected independently of control of power supply to the pixel area, in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and to supply power to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion, as recited by amended Claim 1. In addition, the citations

to Orava et al. and Yamamoto et al. are not understood to disclose or suggest a control circuit configured to effect control to supply power of a second power level to a common output portion (of a plurality of pixels each having a photoelectric conversion portion and the common output portion) in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and supply the first power level, higher than the second power level, to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion

Rather, the Orava et al. patent is understood to disclose addressing logic that comprises means for connecting output lines of the pixel circuits to an output of the imaging device, means for supplying read enable signals to read enable inputs of the pixel circuits, and means for supplying reset signals to reset inputs of the pixel circuits, as discussed at column 5, lines 33-38. As is admitted in the Office Action, this patent fails to disclose or suggest the power supply unit or the control circuit recited by Claim 1. For that reason, the Office Action cites the Yamamoto et al. patent. The Office Action cites column 2, lines 32-46 and column 7 lines 49-60 and Fig. 11 as showing the power supply unit configured to effect power supply control of the common output portion independently of control of the power supply to the pixel area, as recited by Claim 1. But, neither column 2, lines 32-46, nor column 7, lines 49-60 is understood to discuss that a power supply unit is configured to effect power supply control of the common output portion independently of control of the power supply to the pixel area as can be seen by reviewing these portions of the Yamamoto et al. patent, which are reproduced below:

> In another aspect of the present invention, there is provided an image sensor comprising a control circuit for repeating sequential operation of a light integration period, a read-out period and a power-off period, wherein the control circuit: in

> the light integration period, causes the pixel array to perform light integration without supplying power to the read-out circuit; in the read-out period, causes the read-out circuit to read out the integrated signals; and in the power-off period, ceases to supply power to the pixel array and the read-out circuit.
>
> With this aspect, power supply for the read-out circuit ceases in the light integration period and besides, power supply to the pixel array and the read-out circuit ceases in the power-off period, thereby power consumption in the image sensor can be reduced.
>
> . . . .
>
> A mode signal MODE is provided to the power source circuit 21, and the power source circuit 21 supplies power source voltages to circuits at all times when the mode signal indicate a normal mode. The power source circuit 21 supplies the power source voltage to a block BL1 during an enable signal EN1 from a power source control circuit 22 is active and ceases the supply during the signal EN1 is inactive, while supplying the power source voltages to a block BL2 during an enable signal EN2 from the power source control circuit 22 is active and ceases the supply during the signal EN2 is inactive.

In other words, Figure 11 and column 7, lines 49-60 are understood to merely show 1) a supply power circuit 21 supplying voltage to a block BL1 in a light integration period and to the block BL1 and a block BL2 in a reading-out period, 2) the block BL1 including a pixel array 10 and a vertical scanning circuit 11, and 3) the block BL2 including a sample-hold control circuit 13, a sample-hold circuit 14, a horizontal scanning circuit 15, an amplification circuit 17, and an A/D conversion circuit 18. There does not appear to be any reference in these passages to a power supply unit configured to effect power supply control of the common output portion independently of control of the power supply to a pixel area.

In addition, the Office Action cites column 8, lines 44-54 of the Yamamoto et al. as showing the claimed control circuit of Claims 1 and Claim 4. But this passage is not understood to disclose or suggest a control circuit configured to effect control to supply no power to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and to supply power to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion, as recited by Claim 1, or a control circuit configured to effect control to supply power of the second power level to the common output portion in a predetermined period after starting photo-charge accumulation in the photoelectric conversion portion and supply the first power level to the common output portion before the end of a photo-charge accumulation period in the photoelectric conversion portion, as recited by Claim 4, as can be seen by reviewing this passage:

> In response to the rising edge of a vertical sync signal VSYNC, the count of the counter 23 becomes 1 and the enable signal EN2 goes high and the power source voltages are also supplied to the block BL2.
>
> In the block BL1, the pixel lines are sequentially activated and the vertical read out and resetting are performed line by line. In the block BL2, the horizontal read out is performed each time after pixel signals from selected one row are latched in the sample and hold circuits 14.
>
> That is, operation in the read out period is the same as that in the normal mode.

Since the cited art is not understood to disclose or suggest all the features of Claims 1 and 4, Applicant submits that the Office has not yet satisfied its burden of proof to establish a prima facie case of obviousness against Claims 1 and 4. For this reason, Applicant respectfully requests that the rejection of Claims 1 and 4 be withdrawn.

The dependent claims are also submitted to be patentable, due to their dependency from the independent base claims, as well as due to additional features that are recited. Individual consideration of the dependent claims is respectfully solicited.

Conclusion

In view of the above amendments and remarks, the application is now in allowable form. Therefore, early passage to issue is respectfully solicited.

Any fee required in connection with this paper should be charged to Deposit Account No. 06-1205.

Applicant's undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,

/Gary M. Jacobs/

Gary M. Jacobs
Attorney for Applicant
Registration No. 28,861

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200
GMJ/klm

FCHS_WS 2165890v1